WHAT IS CLAIMED IS:

1. A circuit for providing an indication that a signal level of a primary power source transitions below a predefined threshold level, the circuit comprising:

a first transistor electrically coupled to a second transistor, a common node being formed along the coupling;

a third transistor having a gate terminal coupled to the common node; and

at least one pair of series connected trimming transistors, a first transistor of the at least one pair of trimming transistors having a gate terminal coupled to the common node, the at least one pair of series connected trimming transistors coupled to a drain/source region of the third transistor.

2. The circuit according to claim 1, further including a fuse electrically coupled to a gate terminal of a second transistor of the at least one pair of trimming transistors, the fuse being blown to selectively turn on/off the second transistor of the at least one pair of trimming transistors.

3. The circuit according to claim 1, wherein the first transistor is coupled to the primary power source and a gate terminal of the second transistor is coupled to a substrate of the circuit.

4. A circuit, comprising:

a first transistor having its source/drain terminals connected between a external power supply voltage and a first node;

a second transistor having its source/drain terminals connected between the first node and a reference voltage, and further having a gate terminal connected to receive a substrate voltage related to a backup supply voltage; and

a third transistor having its source/drain terminals connected between an output node and the reference voltage, and further having a gate terminal connected to the first node.

5. The circuit of claim 4 wherein the first transistor is a p-channel device and the second and third transistors are n-channel devices.

6. The circuit of claim 4 wherein the third transistor drives the output node to change state responsive to a drop in the external power supply voltage below a threshold value.

7. The circuit of claim 6 wherein the threshold value depends on a pull exerted by the first transistor.

8. The circuit of claim 7 further including circuitry for adjusting the pull exerted by the first transistor to effectuate a change in the threshold value.

9. The circuit of claim 8 wherein the circuitry comprises a pair of drain/source terminal series connected transistors which are connected between the external power supply voltage and the output node, a first one of the pair of transistors having its gate terminal connected to the first node and a second one of the pair of transistors having its gate terminal connected to receive a threshold voltage trim control signal.

10. The circuit of claim 8 wherein the circuitry comprises a plurality of pairs of drain/source terminal series connected transistors, each pair being connected between the external power supply voltage and the output node, a first one of the transistors in each pair having its gate terminal connected to the first node and a gate terminal of each second one of the transistors in each pair connected to receive its own threshold voltage trim control signal.

11. The circuit of claim 10 wherein a first subset of the plurality of pairs receive voltage trim control signals to drive the second transistors in each pair to a normally on condition and a second subset of the plurality of pairs receive voltage trim control signals to drive the second transistors in each pair to a normally off condition.

12. The circuit of claim 11 further including a trim selection circuit operable to selectively and individually configure the voltage trim control signals to change the normally on/off condition of the second transistors in each pair.

13. The circuit of claim 12 wherein the trim selection circuit comprises selectively blowable fuse circuitry.

14. The circuit of claim 4 further including pull up circuitry connected between the external power supply voltage and the output node.

15. The circuit of claim 14 wherein the pull up circuitry comprises a pair of drain/source terminal series connected transistors which are connected between the external power supply voltage and the output node, a first one of the pair of transistors having its gate terminal connected to the first node and a second one of the pair of transistors having its gate terminal connected to the reference voltage.

16. A circuit for providing an indication that a voltage of a primary power source transitions below a threshold level, comprising:

a first transistor;

a second transistor electrically coupled to the first transistor at a common node;

a third transistor having a gate terminal coupled to the common node and a conduction terminal at which the indication is produced; and

a pair of series connected threshold level trimming transistors, a first transistor of the pair having a gate terminal coupled to the common node, a second transistor of the pair receiving a threshold level trimming control signal, and the pair being coupled to the conduction terminal at which the indication is produced.

17. The circuit of claim 16, wherein the first transistor is coupled to the primary power source and a gate terminal of the second transistor is coupled to a substrate of the circuit.

18. The circuit of claim 16 wherein the first transistor exerts a pull which sets the threshold level, the pair of series connected threshold level trimming transistors adjusting the pull exerted by the first transistor in response to the threshold level trimming control signal to effectuate a change in the threshold level.

19. The circuit of claim 16 further including pull up circuitry connected between the external power supply voltage and the conduction terminal at which the indication is produced.

20. The circuit of claim 19 wherein the pull up circuitry comprises a pair of drain/source terminal series connected transistors which are connected between the external power supply voltage and the conduction terminal at which the indication is produced, a first one of the pair of transistors having its gate terminal connected to the first node and a second one of the pair of transistors having its gate terminal connected to the reference voltage.